

Home | Login | Logour | Access information | Alt

Search	Results	
Searcn	Kesuits	

	RESEASE 2.1		61	resconse unice amie	is ratemany ()	ademark Since		
Search Resu	its '			erowse	S	EARCH	IEEE XPLORE GUIDE	•
Your search	((((((reconfig*, configur*) <and> matched 46 of 438 documents. of 100 results are displayed, 25 to</and>							☑ e-mail
» Search Opt	ions	Modify	Sec	ırch				
View Session	n History	((((((re	conf	g*, configur*) <and> (pi</and>	ipe*)) <in>metadat</in>	a)) <and>(different * d</and>	or distinct Search >	
New Search		. c	hec	to search only within	this results set			
		Display				Citation & Abstract		
» Key								
eene jal	IEEE Journal or Magazine	r vier	N 5	elected items	Select All Des	select All		
iee Jnl	IEE Journal or Magazine			•				
HEER CAP	IEEE Conference Proceeding	, 🗀	1.	The flexibility of cor Villasenor, J.; Hutchin	-	puting	,	
iee Cnf	IEE Conference Proceeding			Signal Processing Ma	=		•	-
CY2 3331	IEEE Standard			Volume 15, Issue 5, Digital Object Identific				
	÷			AbstractPlus Full Te Rights and Permission	ext: <u>PDF(</u> 5100 K			
			2.	Lodi, A.; Toma, M.; C Solid-State Circuits. J Volume 38, Issue 11 Digital Object Identific AbstractPlus Refere Rights and Permission	Campi, F.; Cappe IEEE Journal of I, Nov. 2003 Pag er 10.1109/JSSC ences Full Text:	elli, A.; Canegallo, F ge(s):1876 - 1886 C.2003.818292		ns
•			3.	Implementing an Off Ebeling, C.; Fisher, C Computers, JEEE Tra Volume 53, Issue 11 Digital Object Identific AbstractPlus Refere Rights and Permission	C.; Guanbin Xing ansactions on I, Nov. 2004 Pag er 10.1109/TC.2 ances Full Text:	; Manyuan Shen; F ge(s):1436 - 1448 004.98		
	•	n	4.	A configurable pipe Zipf, P.; Stotzler, C.; VI.SI: 2004 Proceed 19-20 Feb. 2004 Pag AbstractPius Full Te Rights and Permission	Glesner, M.; lings !EEE Comi ge(s):266 - 267 ext: <u>PDF(</u> 214 KB	outer society Annu:	ASIC and configurable arc al Symposium on	hitecture
	·	Ď	5.	Campi, F.; Cappelli,	A.; Guerrieri, R.; ted Processing S ge(s):8 pp.	Lodi, A.; Toma, M. ymposium, 2003. F	re development environme ; La Rosa, A.; Lavagno, L.; l Proceedings_international	

AbstractPlus | Full Text: PDF(267 KB) | III EE CNF

Rights and Permissions

	6.	A methodical approach for stream-oriented configurable signal processing Swanchara, S.; Athanas, P.; System Sciences, 1999. HICSS-32. Proceedings of the 32nd Annual Hawaii International Conferent Volume Track3, 5-8 Jan. 1999 Page(s):6 pp. Digital Object Identifier 10.1109/HICSS.1999.772884
		AbstractPlus Full Text: PDF(56 KB) 注题ECNF Rights and Permissions
	7.	A programmable digital neuro-processor design with dynamically reconfigurable pipeline/pa Young-Jin Jang; Chan-Ho Park; Hyon-Soo Lee; Parallel and Distributed Systems, 1998. Proceedings, 1998 International Conference on 14-16 Dec. 1998 Page(s):18 - 24 Digital Object Identifier 10.1109/ICPADS.1998.741014 AbstractPlus Full Text: PDE(1016 KB) IEEE CRF
		Rights and Permissions
	8.	An ATM application specific integrated processor Harasawa, A.; Kaganoi, T.; Kanoh, T.; Nishizaki, H.; Suzuki, M.; Tomizawa, H.; Shindou, T.; Custom Integrated Circuits Conference. 1997. Proceedings of the IEEE 1997 5-8 May 1997 Page(s):445 - 448 Digital Object Identifier 10.1109/CICC.1997.606663 AbstractPlus Full Text: PDF(468 KB) III EXT. CNIF Rights and Permissions
	9.	Streaming processors for next-generation mobile imaging applications Chai, S.M.; Chiricescu, S.; Essick, R.; Lucas, B.; May, P.; Moat, K.; Norris, J.M.; Schuette, M.; Lope Communications Magazine. IEEE Volume 43, Issue 12, Dec. 2005 Page(s):81 - 89 Digital Object Identifier 10.1109/MCOM.2005.1561924 AbstractPlus Full Text: PDE(276 KB) 18:000 JNE. Rights and Permissions
	10.	Code size reduction in heterogeneous-connectivity-based DSPs using instruction set extensed Biswas, P.; Dutt, N.D.; Computers. IEEE Transactions on Volume 54, Issue 10, Oct. 2005 Page(s):1216 - 1226 Digital Object Identifier 10.1109/TC.2005.157 AbstractPlus Full Text: PDE(1152 KB) IEEE JNL Rights and Permissions
	11.	Resynchronization for multiprocessor DSP systems Bhattacharyya, S.S.; Sriram, S.; Lee, E.A.; Circuits and Systems I: Fundamental Theory and Applications. IEEE Transactions on [see also Circuits and Systems II: Fundamental Theory and Applications. IEEE Transactions on [see also Circuits and Papers. IEEE Transactions on] Volume 47, Issue 11, Nov. 2000 Page(s):1597 - 1609 Digital Object Identifier 10.1109/81.895327 AbstractPlus References Full Text: PDE(264 KB) IEEE JNL Rights and Permissions
	12.	Reconfigurable parallel inner product processor architectures Rong Lin; Very Large Scale Integration (VLSI) Systems IEEE Transactions on Volume 9, Issue 2, April 2001 Page(s):261 - 272 Digital Object Identifier 10.1109/92.924037 AbstractPlus References Full Text: PDE(340 KB) IEEE JNL Rights and Permissions

•	B. FPGA prototyping of a RISC processor core for embedded applications Gschwind, M.; Salapura, V.; Maurer, D.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 9, Issue 2, April 2001 Page(s):241 - 250 Digital Object Identifier 10.1109/92.924027	
	AbstractPlus References Full Text: PDF(436 KB) IEEE JNL Rights and Permissions	
	Se-Jeong Park; Jeong-Su Kim; Ramchan Woo; Se-Joong Lee; Kang-Min Lee; Tae-Hum Y Yoo; Solid-State Circuits. IEEE Journal of Volume 37, Issue 5, May 2002 Page(s):612 - 623 Digital Object Identifier 10.1109/4.997855	
	AbstractPlus References Full Text: PDF(484 KB)	
•	Zyuban, V.; Yery Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 11, Issue 5, Oct 2003 Page(s):778 - 788 Digital Object Identifier 10.1109/TVLSI.2003.814322 AbstractPlus References Full Text: PDF(903 KB) ISSES JNL. Rights and Permissions	
	S. Programmable stream processors Kapasi, U.J.; Rixner, S.; Dafly, W.J.; Khailany, B.; Jung Ho Ahn; Mattson, P.; Owens, J.D.; Computer Volume 36, Issue 8, Aug. 2003 Page(s):54 - 62 Digital Object Identifier 10.1109/MC.2003.1220582	
	AbstractPlus References Full Text: PDF(564 KB)	
1	 7. PITIA: an FPGA for throughput-intensive applications Singh, A.; Mukherjee, A.; Macchiarulo, L.; Marek-Sadowska, M.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 11, Issue 3, June 2003 Page(s):354 - 363 Digital Object Identifier 10.1109/TVLSI.2003.810780	
	AbstractPlus References Full Text: PDF(640 KB) IEEE JAIL Rights and Permissions	
)	Krall, A.; Pryanishnikov, I.; Hirnschrott, U.; Panis, C.; Micro. IEEE Volume 24, Issue 4, July-Aug. 2004 Page(s):67 - 78 Digital Object Identifier 10.1109/MM.2004.40	
	AbstractPlus References Full Text: PDF(184 KB)	
1	O. A method for designing high-radix multiplier-based processing units for multimedia Guevorkian, D.; Launiainen, A.; Lappalainen, V.; Liuha, P.; Punkka, K.; Circuits and Systems for Video Technology, IEEE Transactions on Volume 15, Issue 5, May 2005 Page(s):716 - 725 Digital Object Identifier 10.1109/TCSVT.2005.846436	applical
	AbstractPlus References Full Text: PDE(1144 KB) IEIEE UNI. Rights and Permissions	
1). Computation of prime factor DFT and DHT/DCCT algorithms using cyclic and skew-	cvelie bř

	IC convolvers Gudvangen, S.; Holt, A.G.J.; <u>Circuits Devices and Systems. IEE Proceedings G</u> Volume 137, Issue 5, Oct. 1990 Page(s):373 - 389 <u>AbstractPlus Full Text: PDF(976 KB) III EUNE</u>
	21. Design and Implementation of an Embedded Microprocessor Compatible with IL Language in Norm IEC 61131-3 Carrillo, S.; Polo, A.; Esmeral, M.; Reconfigurable Computing and FPGAs, 2005. ReConFig 2005. International Conference on 28-30 Sept. 2005 Page(s):23 - 23 Digital Object Identifier 10.1109/RECONFIG.2005.14
,	AbstractPlus Full Text: PDF(232 KB) ###################################
	22. A programmable DSP architecture for wireless communication systems Kamalizad, A.; Tabrizi, N.; Bagherzadeh, N.; Hatanaka, A.; Application-Specific Systems, Architecture Processors, 2005, ASAP 2005, 16th IEEE International 23-25 July 2005 Page(s):231 - 238 Digital Object Identifier 10.1109/ASAP.2005.9
	AbstractPlus Full Text: <u>PDF(</u> 288 KB) ISSE CNF Rights and Permissions
	23. An FPGA-Based Floating-Point Jacobi Iterative Solver Morris, G.R.; Prasanna, V.K.; Parallel Architectures Algorithms and Networks, 2005. ISPAN 2005. Proceedings, 8th International 07-09 Dec. 2005 Page(s):420 - 427 Digital Object Identifier 10.1109/ISPAN.2005.18 AbstractPlus Full Text: PDE(320 KB) ISEE CNF
	Rights and Permissions
	24. Functionality Distribution for Parallel Rendering Rajagopalan, R.; Goswami, D.; Mudur, S.P.; Parallel and Distributed Processing Symposium, 2005. Proceedings. 19th IEEE International 04-08 April 2005 Page(s):18 - 18 Digital Object Identifier 10.1109/IPDPS.2005.232 AbstractPlus Full Text: PDF(288 KB) IEEE CNF Rights and Permissions
	25. Resource sharing and pipelining in coarse-grained reconfigurable architecture for domain-s Yoonjin Kim; Kiemb, M.; Park, C.; Jinyong Jung; Kiyoung Choi;

Design, Automation and Test in Europe, 2005. Proceedings

Digital Object Identifier 10.1109/DATE.2005.260

AbstractPlus | Full Text: PDF(208 KB)

EEE CNF

2005 Page(s):12 - 17 Vol. 1

Minspec

Help Contact Us Privac

♥ Copyright 2006 Hi



Home | Legin | Legish | Access information | Alc

Welcome United States Patent and Trademark Office

PROVISE

SEARCH

IEEE XPLORE GUIDE

Docute for "II		(nino*)\ <in>n</in>	potadata)/cand/different * or dis **
	((((((reconfig., configur.) <and> natched 46 of 438 documents.</and>	(pipe")) <in>n</in>	netadata)) <and>(different * or dis"</and>
A maximum o	of 46 results are displayed, 25 to a	page, sorted	by Relevance in Descending order.
» Search Options		Modify	y Search
View Session	History	((((((re	econfig*, configur*) <and> (pipe*))<in>metadata))<and>(different * or distinct*<</and></in></and>
New Search			Check to search only within this results set
		Displa	y Format: G Citation C Citation & Abstract
» Key			
IEEE JNL	IEEE Journal or Magazine	← vie	w selected items Select All Deselect All
iee Jnl	IEE Journal or Magazine		
ieee Cnf	IEEE Conference Proceeding		26. SMTp: an architecture for next-generation scalable multi-threading
iee Cnf	IEE Conference Proceeding		Chaudhuri, M.; Heinrich, M.; <u>Computer Architecture, 2004, Proceedings, 31st Annual international Symposium on</u>
CITE SIBB	IEEE Standard		19-23 June 2004 Page(s):124 - 135
	•		Digital Object Identifier 10.1109/ISCA.2004.1310769 AbstractPlus Full Text: PDF(391 KB) IEEE CNF
			Rights and Permissions
		m	27. A field programmable bit-serial digital signal processor
			Rahim, S.A.; Turner, L.E.; System-on-Chip for Real-Time Applications, 2004.Proceedings, 4th IEEE International Workshop o
			19-21 July 2004 Page(s):295 - 298
			AbstractPlus Full Text: PDF(263 KB) ISSE CNF Rights and Permissions
			28. High-level optimization of pipeline design
	,		Campbell, J.P.L.; Day, N.A.; High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International
	•		2003 Page(s):43 - 48
•	· · · · · · · · · · · · · · · · · · ·		Digital Object Identifier 10.1109/HLDVT.2003.1252473 AbstractPlus Full Text: PDE(453 KB) 総部をの解析
			Rights and Permissions
			29. Picking statistically valid and early simulation points
			Perelman, E.; Hamerly, G.; Calder, B.; Parallel Architectures and Compilation Techniques, 2003, PACT 2003, Proceedings, 12th Internatur
			27 Sept1 Oct. 2003 Page(s):244 - 255
			Digital Object Identifier 10.1109/PACT.2003.1238020
			AbstractPlus Full Text: PDF(356 KB) 설립을 다양한 Rights and Permissions
			30. Compiler-generated communication for pipelined FPGA applications
			Ziegler, H.E.; Hall, M.W.; Diniz, P.C.; Design Automation Conference, 2003, Proceedings
			2-6 June 2003 Page(s):610 - 615
			AbstractPlus Full Text: PDF(693 KB) 설문은 CNF Rights and Permissions

	11. Reconfigurable Viterbi decoding using a new ACS pipelining technique	
	Zhu, Y.; Benaissa, M.; Application-Specific Systems, Architectures, and Processors, 2003, Proceedings, IEEE Internated 24-26 June 2003 Page(s):360 - 368	ion;
	AbstractPlus Full Text: PDF(265 KB) ISSE CRF Rights and Permissions.	
.	22. Unified radix-4 multiplier for GF(p) and GF(2_n) Au, LS.; Burgess, N.; Application-Specific Systems, Architectures, and Processors, 2003, Proceedings, IEEE Internat 24-26 June 2003 Page(s):226 - 236	ion:
	AbstractPlus Full Text: PDE(331 KB) ISSE CRF Rights and Permissions	
	I3. Branch predictor design and performance estimation for a high performance embedded is Sang-hyuk Lee; II-kwan Kim; Choi, L.; Design Automation Conference. 2003. Proceedings of the ASP-DAC 2003. Asia and South Pac 21-24 Jan. 2003 Page(s):519 - 522 Digital Object Identifier 10.1109/ASPDAC.2003.1195072 AbstractPlus Full Text: PDE(492 KB) ISES CNF	
	Rights and Permissions	
	44. Coarse-grain pipelining on multiple FPGA architectures Ziegler, H.; Byoungro So; Hall, M.; Diniz, P.C.; Field-Programmable Custom Computing Machines, 2002, Proceedings, 10th Annual IEEE Sym 22-24 April 2002 Page(s):77 - 86 Digital Object Identifier 10.1109/FPGA.2002.1106663	ROS
	AbstractPlus Full Text: PDF(1941 KB) IEEE CNF Rights and Permissions	
	55. Automatic verification of in-order execution in microprocessors with fragmented pipeline functional units Mishra, P.; Tomiyama, H.; Dutt, N.; Nicolau, A.; Design. Automation and Test in Europe Conference and Exhibition. 2002. Proceedings 4-8 March 2002 Page(s):36 - 43 Digital Object Identifier 10.1109/DATE.2002.998247	es a
	AbstractPlus Full Text: PDF(348 KB) (SEE CNF Rights and Permissions	
	16. Architecture exploration of parameterizable EPIC SOC architectures Halambe, A.; Cornea, R.; Grun, P.; Dutt, N.; Nicolau, A.; Design, Automation and Test in Europe Conference and Exhibition 2000, Proceedings 27-30 March 2000 Page(s):748 Digital Object Identifier 10.1109/DATE.2000.840881	
	AbstractPlus Full Text: PDF(20 KB) IEEE CNF Rights and Permissions	
	57. Decoupling local variable accesses in a wide-issue superscalar processor Sangyeun Cho; Pen-Chung Yew; Gyungho Lee; Computer Architecture, 1999. Proceedings of the 26th International Symposium on 2-4 May 1999 Page(s):100 - 110 Digital Object Identifier 10.1109/ISCA.1999.765943	
	AbstractPlus Full Text: PDE(796 KB) (\$1535 CNF) Rights and Permissions	
	18. Application of reconfigurable CORDIC architectures Mencer, O.; Semeria, L.; Morf, M.; Delosme, JM.; Signals, Systems & Computers, 1998, Conference Record of the Thirty-Second Asilomar Confe	eten

Digital Object Identifier 10.1109/ACSSC.1998.750850 AbstractPlus | Full Text: PDE(416 KB) IMME CNF Rights and Permissions 39. A scaleable FIR filter using 32-bit floating-point complex arithmetic on a configurable comρι Walters, A.; Athanas, P.; FPGAs for Custom Computing Machines, 1998, Proceedings, IEEE Symposium on 15-17 April 1998 Page(s):333 - 334 Digital Object Identifier 10.1109/FPGA.1998.707941 AbstractPlus | Full Text: PDF(24 KB) | IEIEIE CINF Rights and Permissions 40. The systolic array genetic algorithm, an example of systolic arrays as a reconfigurable design Bland, I.M.; Megson, G.M.; FPGAs for Custom Computing Machines, 1998, Proceedings, IEEE Symposium on 15-17 April 1998 Page(s):260 - 261 Digital Object Identifier 10.1109/FPGA.1998.707907 AbstractPlus | Full Text: PDE (96 KB) | III EIE CNF Rights and Permissions 41. ASIC design of a microcontroller with power management unit Seung-Il Sonh; Hun-Mo Yang; Jong-Ick Lee; Moon-Key Lee; Semiconductor Conference, 1998, CAS '98 Proceedings, 1998 International Volume 1, 6-10 Oct. 1998 Page(s):159 - 162 vol.1 Digital Object Identifier 10.1109/SMICND.1998.732324 AbstractPlus | Full Text: PDF(352 KB) IEEE CNF Rights and Permissions 42. Effect of architecture configuration on software reliability and performance estimation Mei-Hwa Chen; Mei-Huei Tang; Wen-Li Wang; Application-Specific Software Engineering Technology, 1998. ASSET-98. Proceedings, 1998 IEEE 26-28 March 1998 Page(s):90 - 95 Digital Object Identifier 10.1109/ASSET.1998.688240 AbstractPlus | Full Text: PDF(168 KB) IEEE CRF Rights and Permissions 43. ATM traffic shaper: ATS Diaz, J.C.; Plaza, P.; Crespo, J.; Design, Automation and Test in Europe, 1998, Proceedings 23-26 Feb. 1998 Page(s):96 - 101 Digital Object Identifier 10.1109/DATE.1998.655842 AbstractPlus | Full Text: PDF(400 KB) ISSE CNF Rights and Permissions 44. Two widely-different architectural approaches to computer image generation Park, H.W.; Eo, K.S.; Kim, D.L.; Choi, B.K.; Kim, Y.; Alexander, T.; Visualization, 1991, Visualization '91, Proceedings, IEEE Conference on 22-25 Oct. 1991 Page(s):42 - 49 Digital Object Identifier 10.1109/VISUAL.1991.175776 AbstractPlus | Full Text: PDF(688 KB) ISSE CNF Rights and Permissions 45. Generating synchronous timed descriptions of digital receivers from dynamic data flow syst configuration Zepter, P.; Grotker, T.; European Design and Test Conference, 1994, EDAC. The European Conference on Design Autom Test Conference, EUROASIC, The European Event in ASIC Design, Proceedings.

Volume 1, 1-4 Nov. 1998 Page(s):182 - 186 vol.1

28 Feb. - 3 March 1994 Page(s):672

Digital Object Identifier 10.1109/EDTC.1994.326923

AbstractPlus | Full Text: PDF(80 KB) ### CNF

Rights and Permissions

46. Application-specific Heterogeneous Multiprocessor Synthesis using Extensible Processors

Sun Fei ; Ravi Srivaths ;

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems : Accepted for fu

Volume PP, Issue 99, 2005 Page(s):1 - 1

Digital Object Identifier 10.1109/TCAD.2005.858269

AbstractPlus | Full Text: PDF(464 KB) | III EIE JNIL

Help Contact Us Priva

& Copyright 2006 (£

